

MS-7407 Ver : 0A

Intel (R) LGA775 Processor (130W)

Intel (R) (GMCH G31) + ICH7 Chipset

CPU:
Intel Core 2 Duo/Extreme/Quad & Pentium D Processor

System Chipset:
Intel G31 (North Bridge) Rev :
Intel ICH7 (South Bridge) Rev :

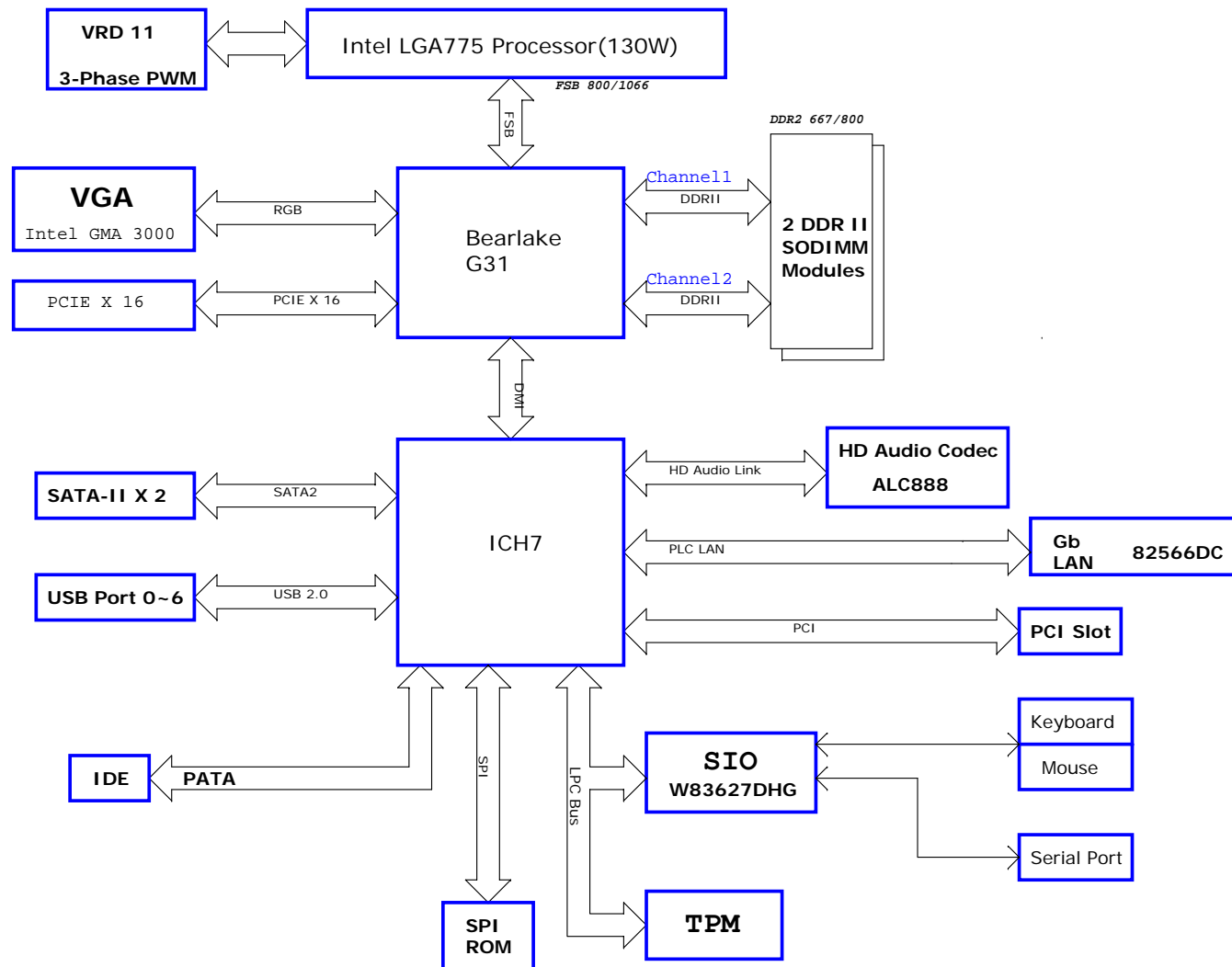
On Board Chipset:
CLOCK : ICS9LP505
PLC LAN ET82566DC
LPC Super I/O : W83627DHG Ver :
Audio Codec : ALC888 7.1 Channel Ver : A1
BIOS : SPI- 16M

Main Memory:
DDR II * 2 (Max 4GB)

Expansion Slots:
PCI X SLOT *1 (FOR PCIE & PCI Riser)

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Block Diagram



Micro Star Restricted Secret		
Title	BLOCK DIAGRAM	Rev 0A
Document Number	MS-7407	
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ICH7

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	ToI	Default	Signal Name
GPIO[0]	BM_BUSY#	AB18	I/O	Vcc3p3	N	Y	3.3	Input	strapped high
GPIO[1]	PCIREQ[5]#	C8	I/O	V5REF	N	Y	5	Input	PREQ#5
GPIO[2]	PIRQE#	G8	I/OD	V5REF	N	Y	5	Input	PIRQ#E
GPIO[3]	PIRQF#	F7	I/OD	V5REF	N	Y	5	Input	PIRQ#F
GPIO[4]	PIRQG#	F8	I/OD	V5REF	N	Y	5	Input	PIRQ#G
GPIO[5]	PIRQH#	G7	I/OD	V5REF	N	Y	5	Input	PIRQ#H
GPIO[6]	unmuxed	AC21	I/O	Vcc3p3	N	Y	3.3	Input	ATADET0
GPIO[7]	unmuxed	AC18	I/O	Vcc3p3	N	Y	3.3	Input	strapped high
GPIO[8]	unmuxed	E21	I/O	VccSus3p3	N	Y	3.3	Input	SIO_PME#
GPIO[9]	unmuxed	E20	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[10]	unmuxed	A20	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[11]	SMBALERT#	B23	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[12]	unmuxed	F19	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[13]	unmuxed	E19	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[14]	unmuxed	R4	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[15]	unmuxed	E22	I/O	VccSus3p3	N	Y	3.3	Input	strapped high
GPIO[16]	unmuxed	AC22	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[17]	PCIGNT[5]#	D8	I/O	Vcc3p3	N	N	3.3	N/A	PGNT#5
GPIO[18]	unmuxed	AC20	I/O	Vcc3p3	N	N	3.3	1	SIO_HOLD#
GPIO[19]	SATA1GP	AH18	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[20]	unmuxed	AF21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[21]	SATA0GP	AF19	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[22]	PCIREQ[4]#	A13	I/O	Vcc3p3	N	N	3.3	Input	PREQ#4
GPIO[23]	LDRQ1#	AA5	I/O	Vcc3p3	N	N	3.3	Input	NC
GPIO[24]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	No Change	LANPHY_DIS#
GPIO[25]	unmuxed	D20	I/O	VccSus3p3	Y	N	3.3	1	DMI_MODE
GPIO[26]	unmuxed	A21	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[27]	unmuxed	B21	I/O	VccSus3p3	N	N	3.3	0	LAN2_EN
GPIO[28]	unmuxed	E23	I/O	VccSus3p3	N	N	3.3	0	NC
GPIO[29]	OC5#	C3	I/O	VccSus3p3	N	N	3.3	Input	USB_OCP#4
GPIO[30]	OC6#	A2	I/O	VccSus3p3	N	N	3.3	Input	USB_OCP#4
GPIO[31]	OC7#	B3	I/O	VccSus3p3	N	N	3.3	Input	USB_OCP#4
GPIO[32]	unmuxed	AG18	I/O	Vcc3p3	N	N	3.3	1	SPI_WP#
GPIO[33]	unmuxed	AC19	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[34]	unmuxed	U2	I/O	Vcc3p3	N	N	3.3	0	NC
GPIO[35]	unmuxed	AD21	I/O	Vcc3p3	N	N	3.3	1	NC
GPIO[36]	SATA2GP	AH19	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[37]	SATA3GP	AE19	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[38]	unmuxed	AD20	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[39]	unmuxed	AE20	I/O	Vcc3p3	N	N	3.3	Input	strapped high
GPIO[48]	GNT4#	A14	I/O	Vcc3p3	N	N	3.3	N/A	PGNT#4
GPIO[49]	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	CPU	N/A	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD20	PCI_CLK1
PCI Slot 2	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD21	PCI_CLK2
1394	PIRQ#B	PREQ#1 PGNT#1	AD19	1394_PCLK

PCI RESET DEVICE

Signals	Target
PCIRST#1	SIO,TPM
PCIRST#2	1394,PCIE X16 SLOT
PCIRST#3	PCI SLOT 1,2
PLTRST#	MS7
HD_RST#	Primary IDE

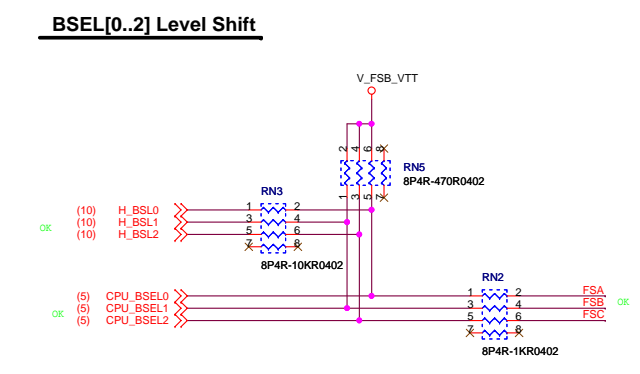
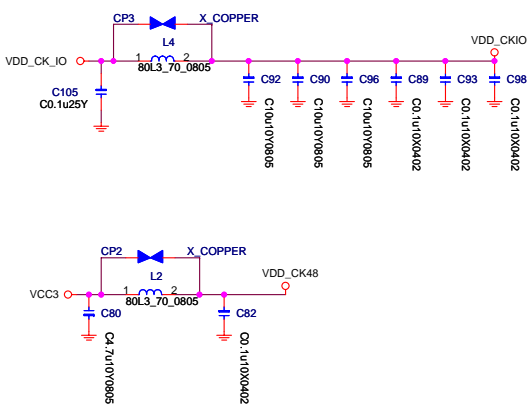
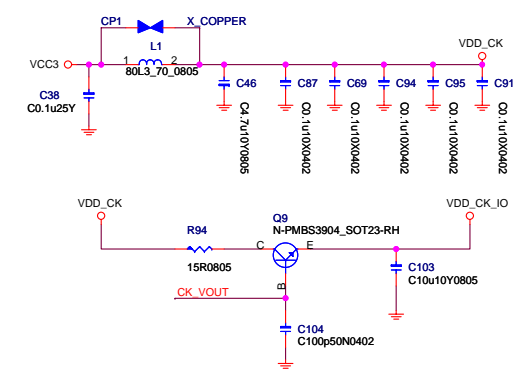
DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	SCLK_A0/SCLK_A#0 SCLK_A1/SCLK_A#1 SCLK_A2/SCLK_A#2
DIMM 2	A2H	SCLK_B0/SCLK_B#0 SCLK_B1/SCLK_B#1 SCLK_B2/SCLK_B#2

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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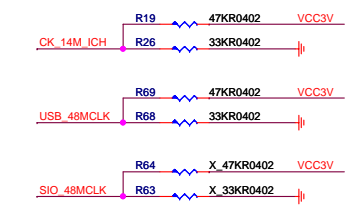
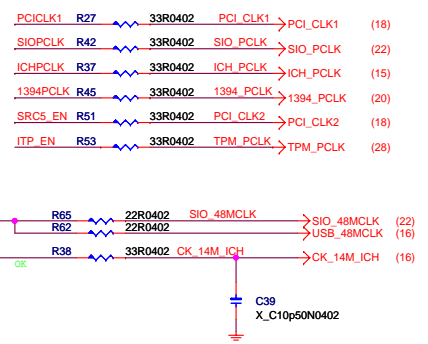
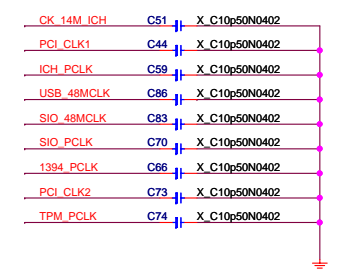
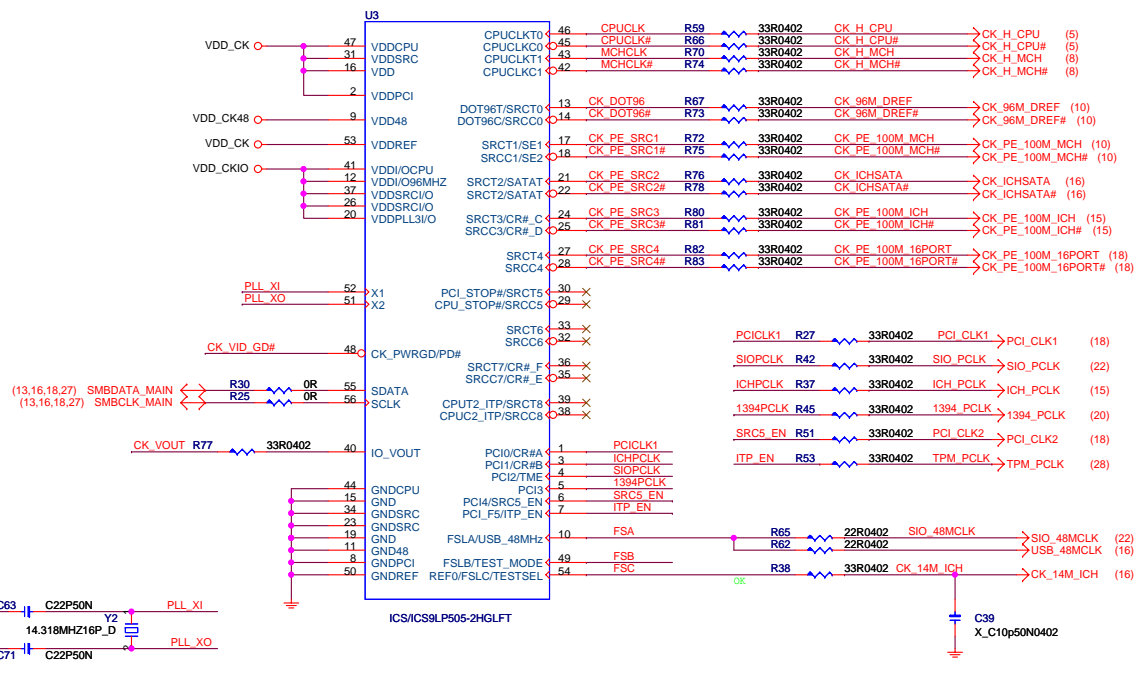
Micro Star Restricted Secret			
Title GPIO & Jumper Setting			Rev 0A
Document Number MS-7407			
MICRO-STAR INT'L CO.,LTD. No. 68, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, May 31, 2007 Sheet 3 of 35	



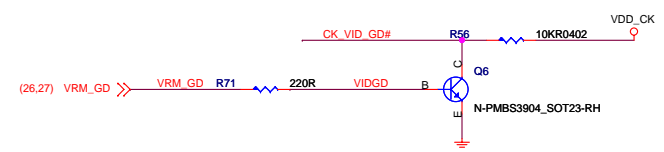
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz (1066)
0 1 0	200 MHz (800)
0 0 1	133 MHz (533)

Clock Generator - ICS9LP505

Trace length less than 0.5inchs



Clock Generator VTT Power Down Block

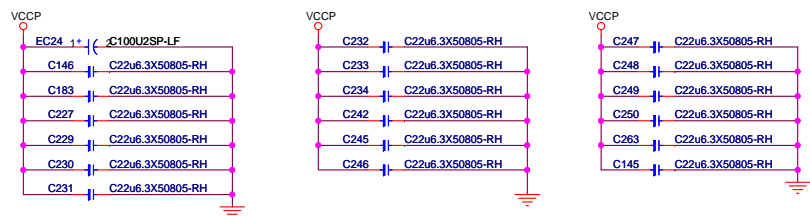


U14C

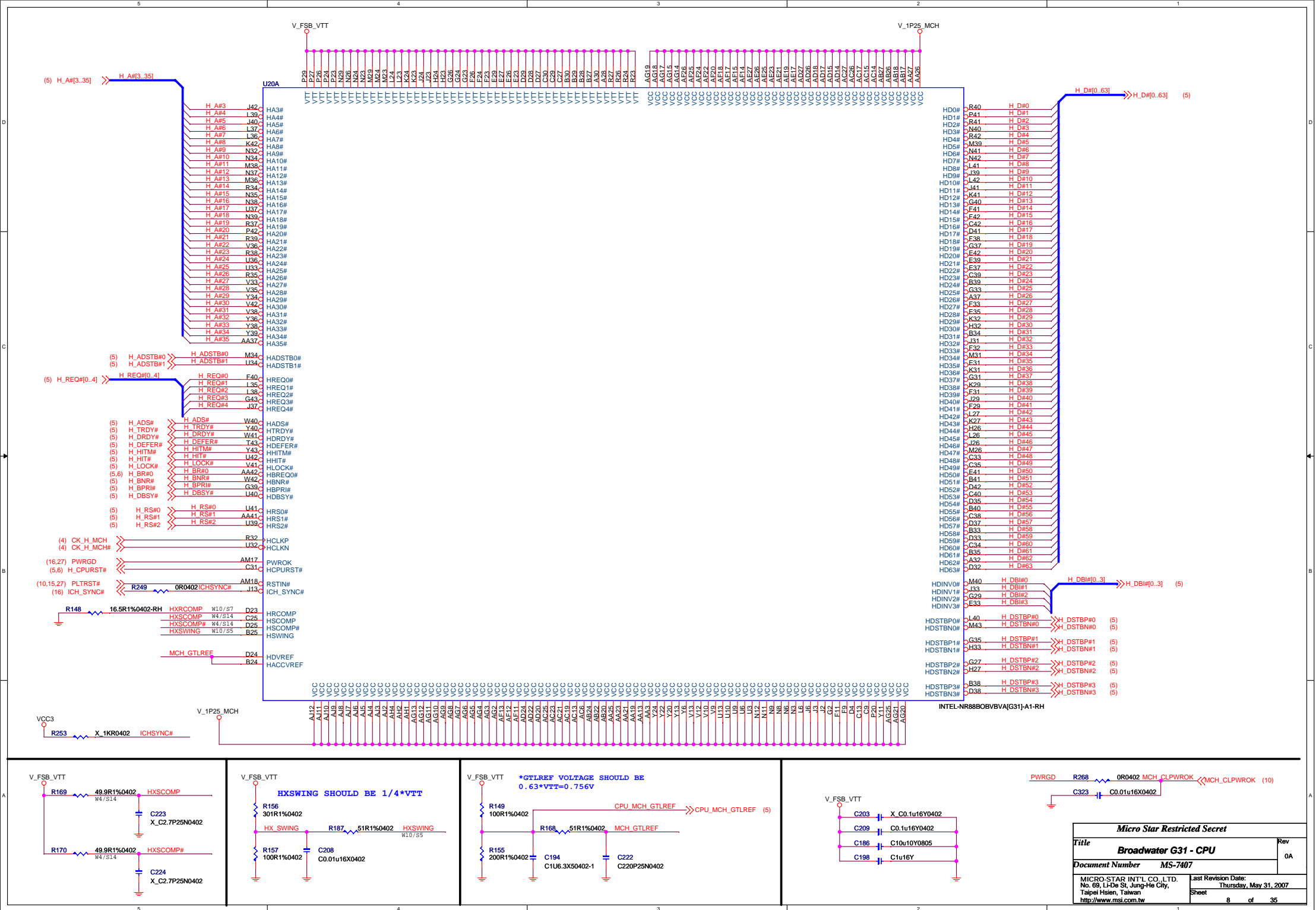
VTT_OUT_RIGHT

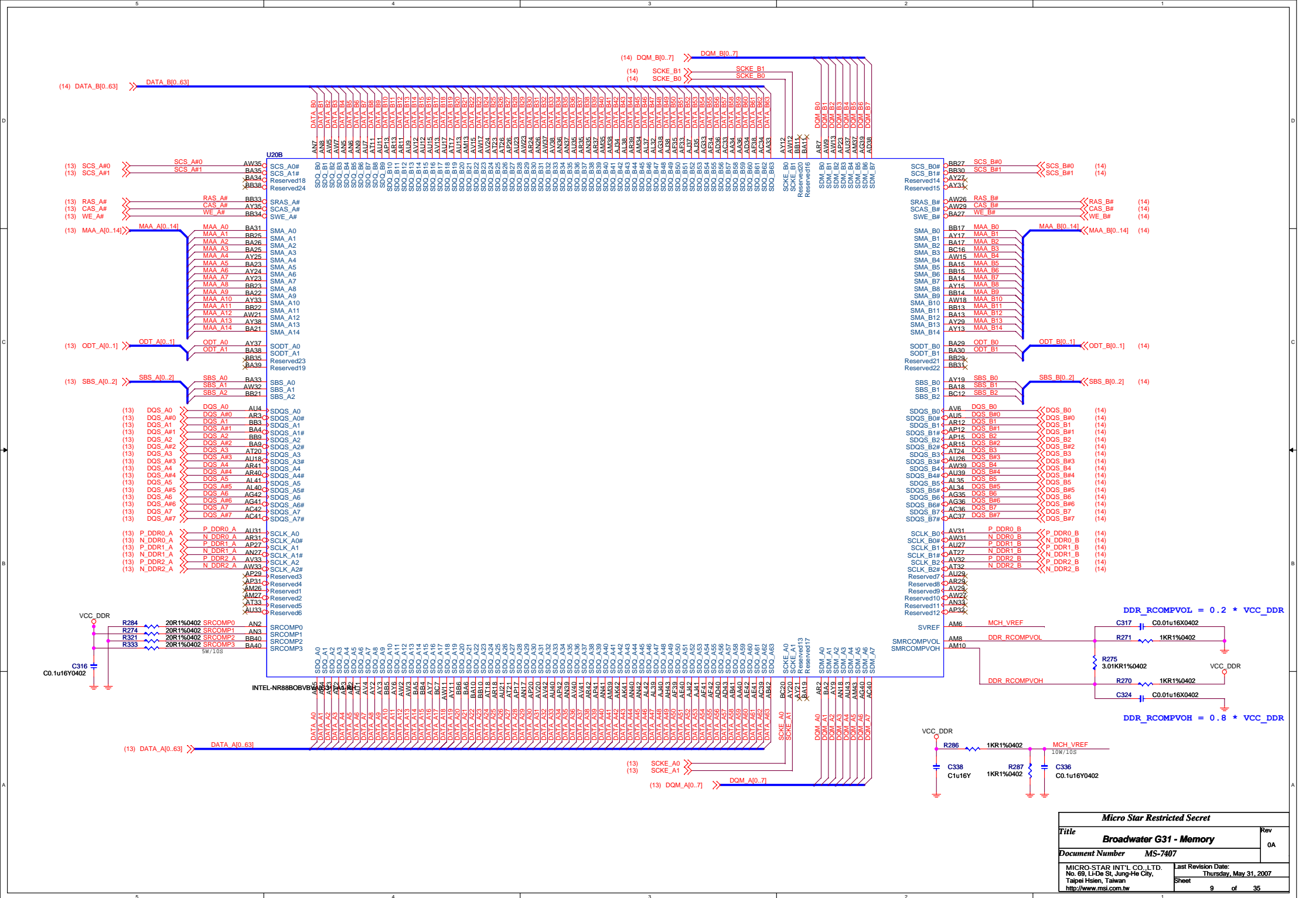
CPU_TP_G1
H_TESTHI_M_U1

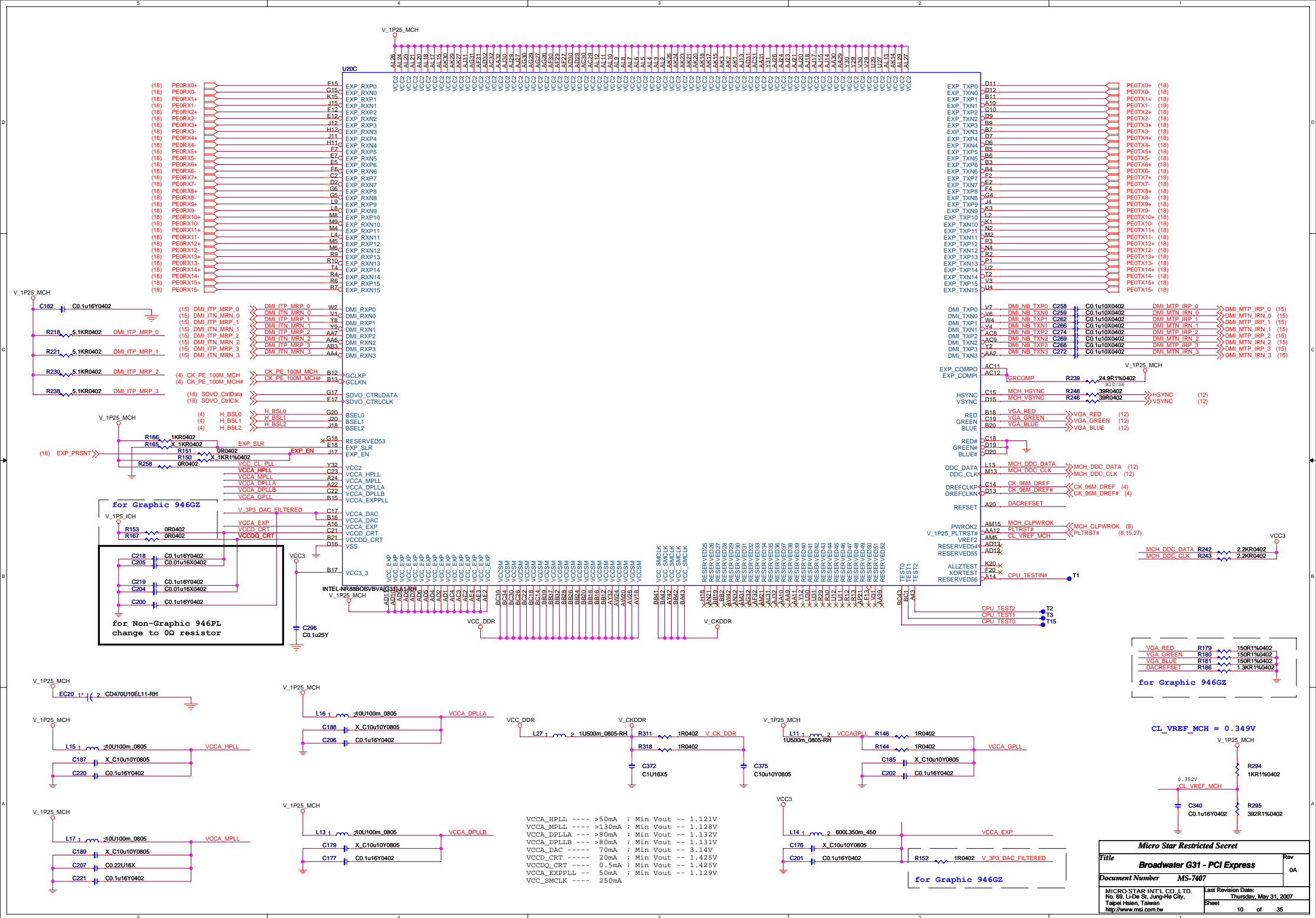
CPU DECOUPLING CAPACITORS



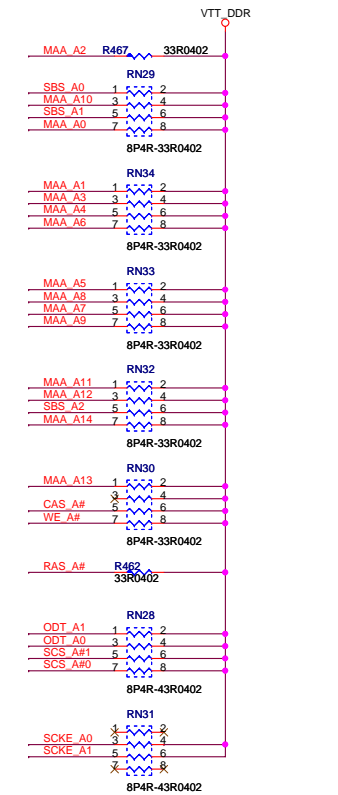
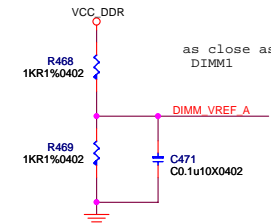
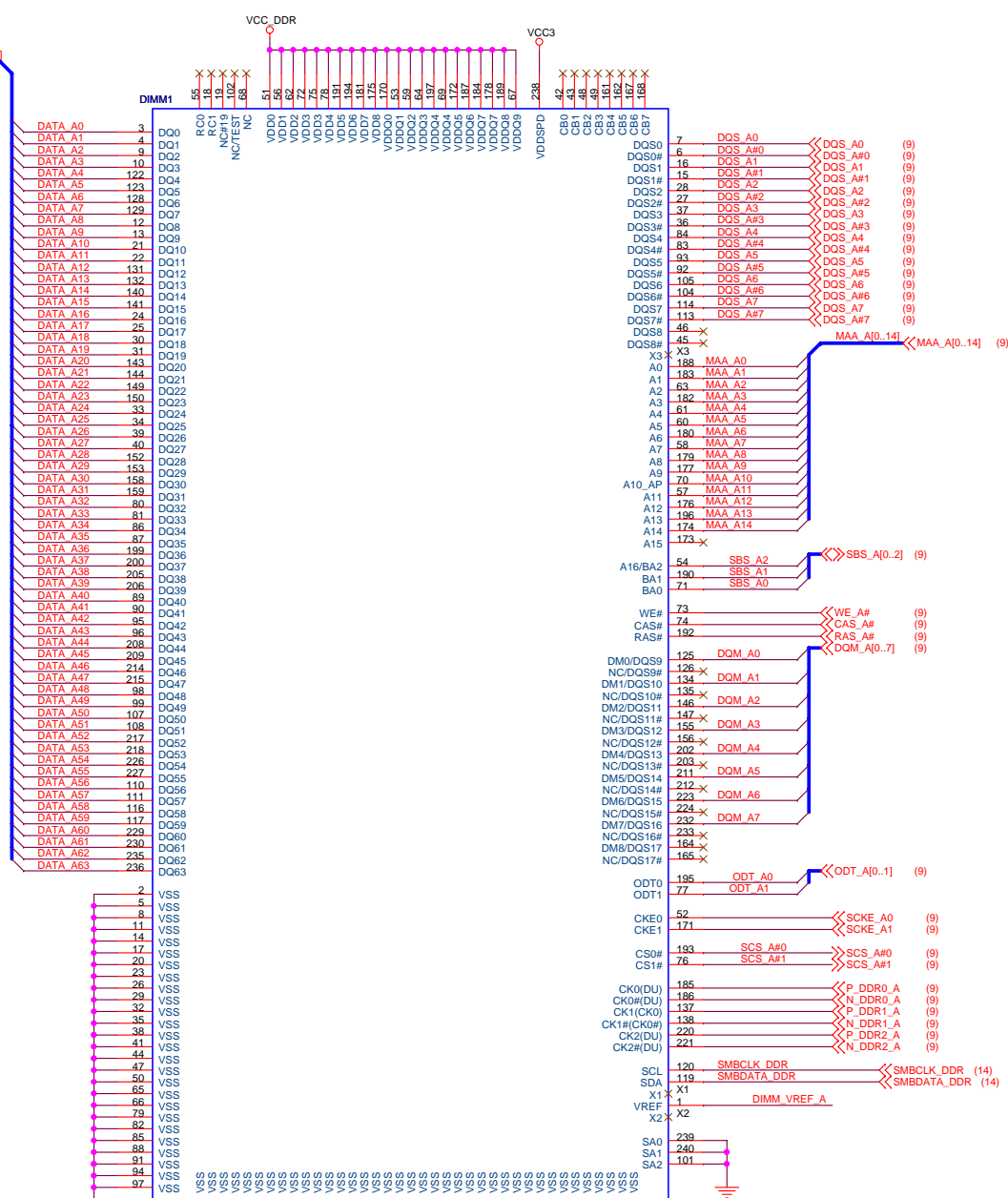
Micro Star Restricted Secret		
Title	Intel LGA775 - GND	Rev 0A
Document Number	MS-7407	
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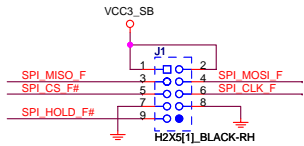
(9) DATA_A[0..63] <<> DATA_A[0..63]



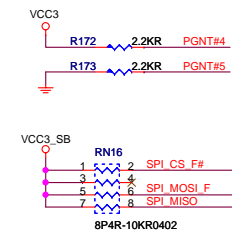
Micro Star Restricted Secret		
Title	DDR II DIMM 1 / Termination	Rev
Document Number	MS-7407	0A
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SPI DEBUG PROT

Place close to SPI ROM

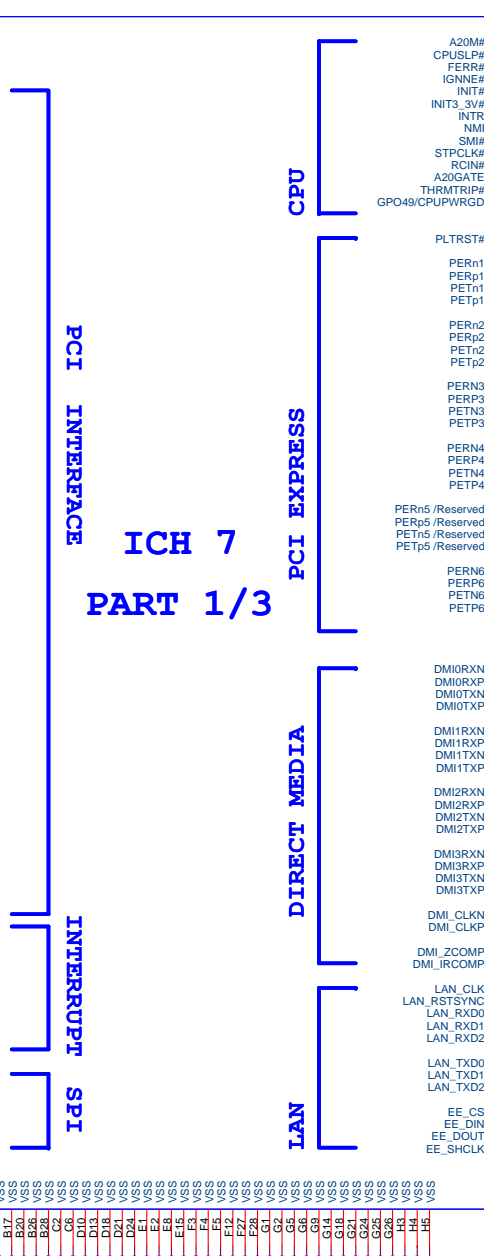
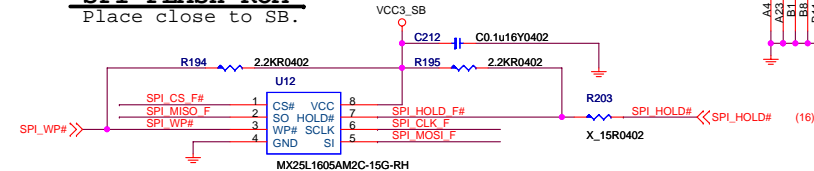


GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC



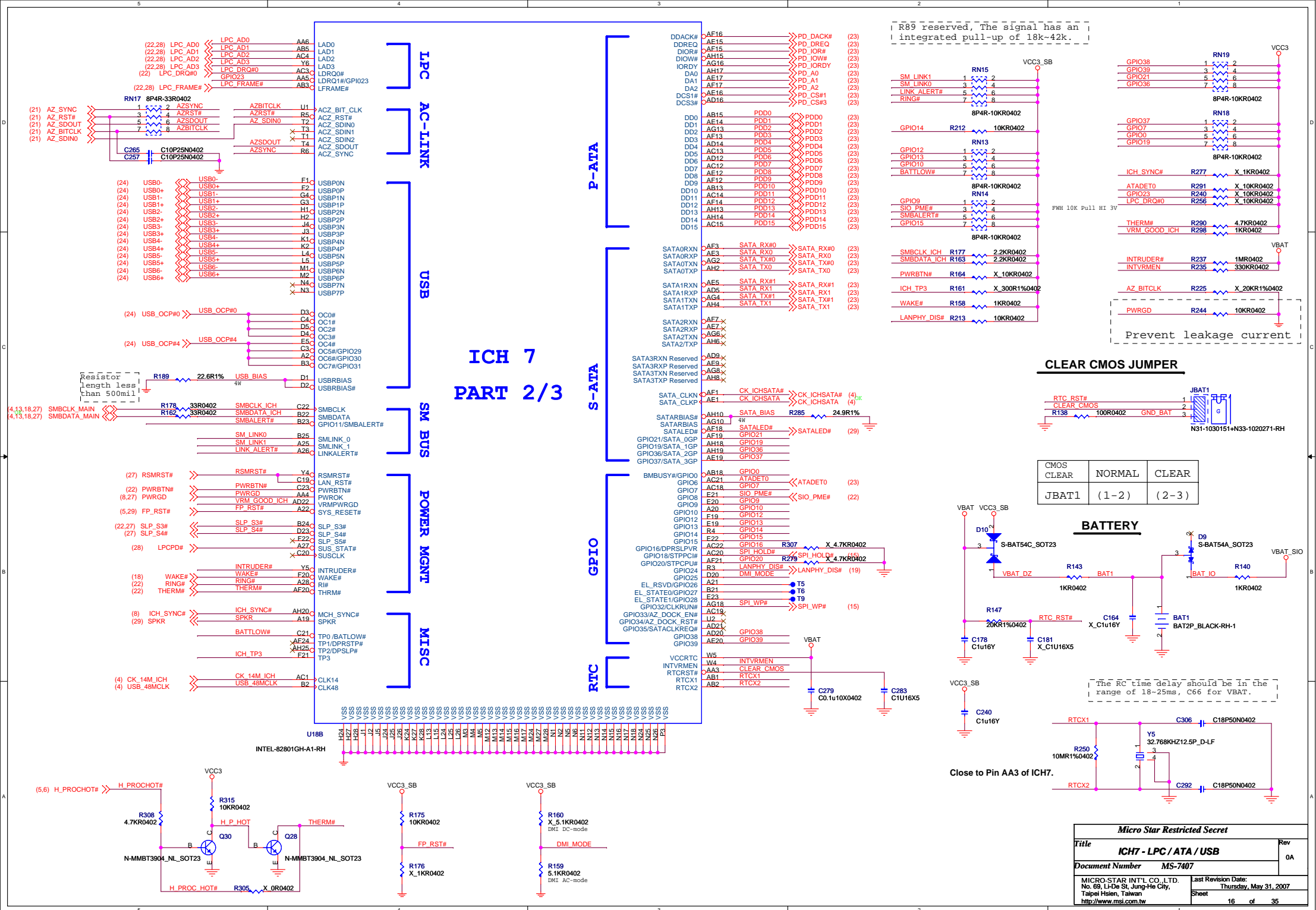
SPI FLASH ROM

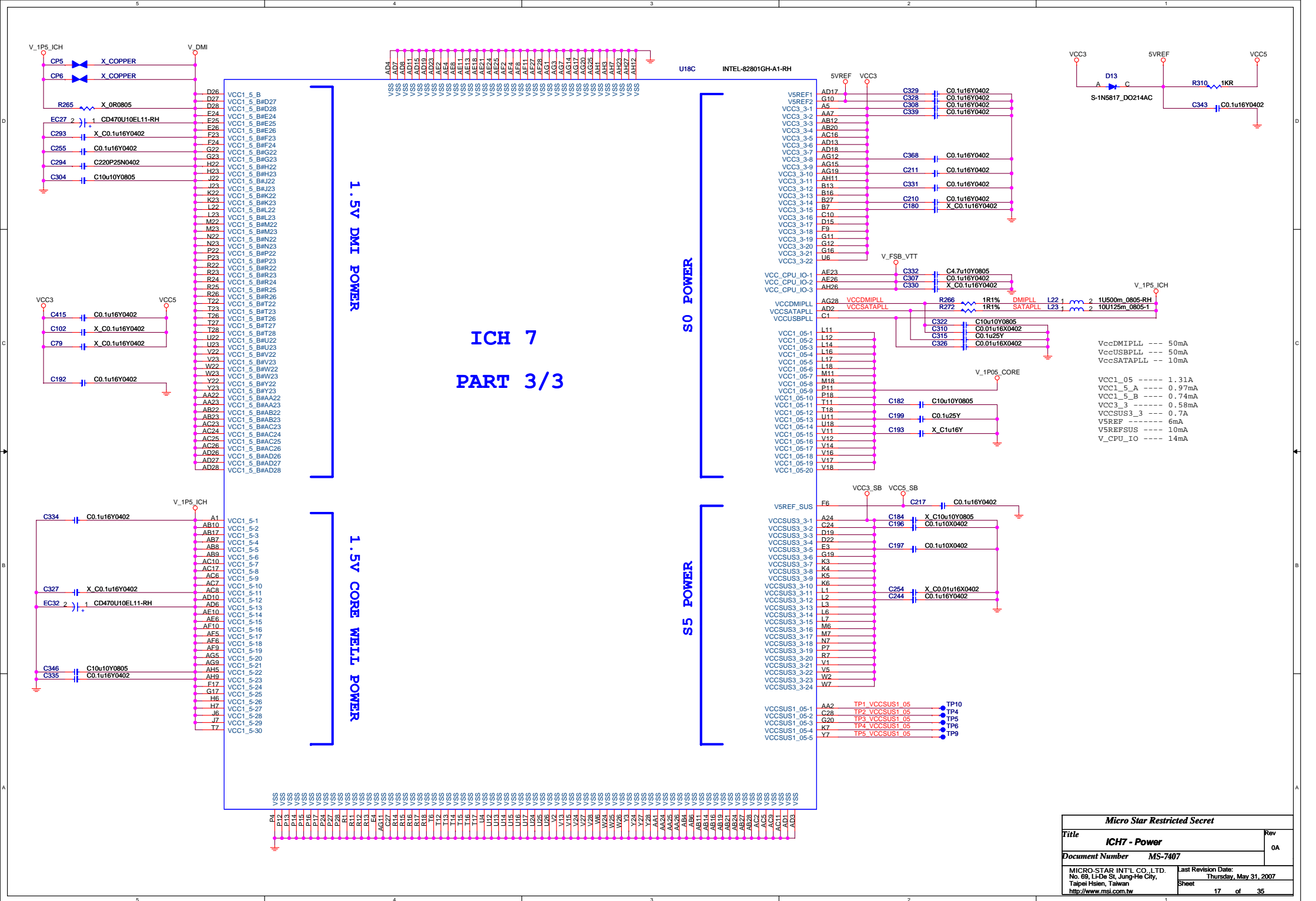
Place close to SB.



Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

Micro Star Restricted Secret		
Title	ICH7 - PCI / DMI / CPU / LAN	Rev
Document Number	MS-7407	QA
MICRO-STAR INT'L CO. LTD.		Last Revision Date:
No. 68, Lihde St, Jung-Ho City,		Thursday, May 31, 2007
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PCI 1

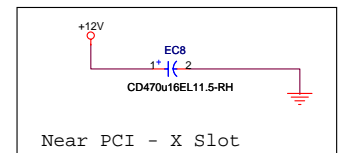
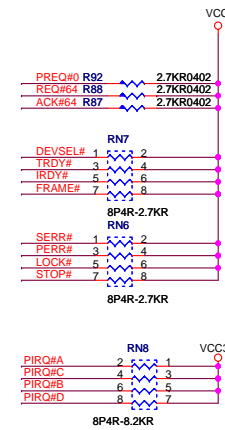
IDSEL: AD20
INT: PIRQ# ABCD
REQ: PREQ#0
GNT: PGNT#0
CLK: PCI_CLK1

PCI 2

IDSEL: AD21
INT: PIRQ# CDAB
REQ: PREQ#2
GNT: PGNT#2
CLK: PCI_CLK2

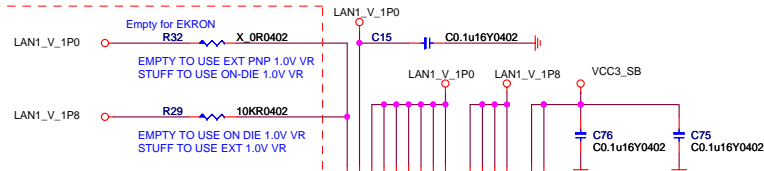
IDSEL R85 100R0402 AD20

PCIRST R90 X_0R0402 PCIRST_ICH# PCIRST_ICH# (15)
PCIRST R91 0R0402 PCIRST#3 PCIRST#3 (27)

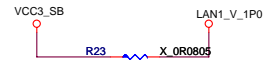


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Title	PCI-X Slot	Rev
Document Number	MS-7407	0A
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NINEVEH 82566DC
EKRON 82562V

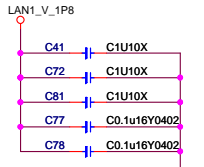
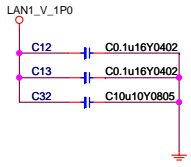
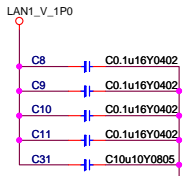
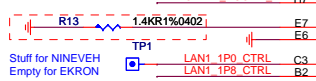
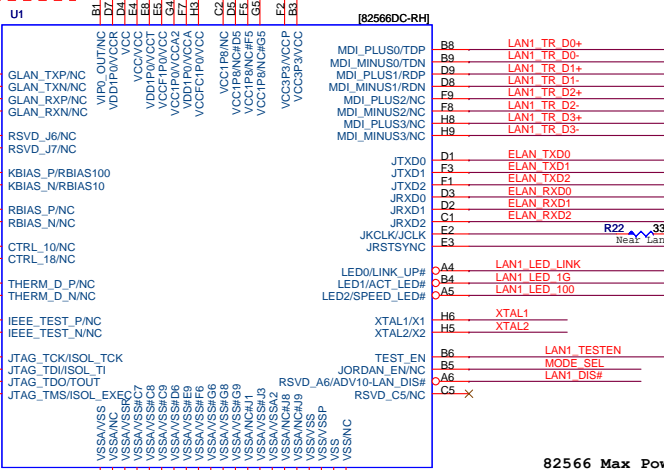
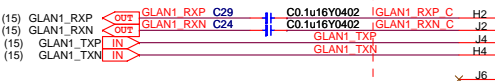


Stuff For EKRON
Empty for NINEVEH

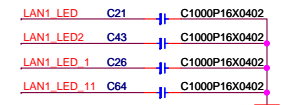
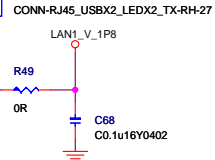
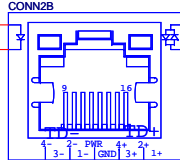
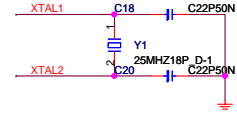


EKRON - 10/100 PHY, LCI
NINEVEH - Gb PHY, GLCI+LCI

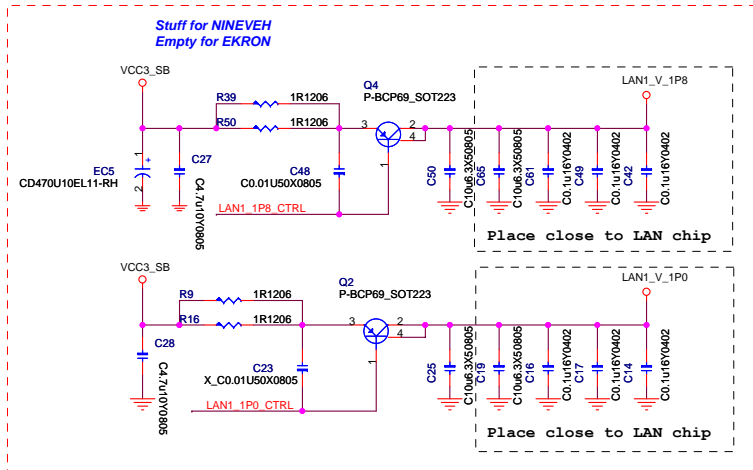
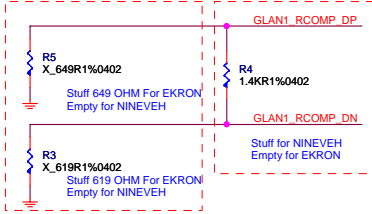
Stuff for NINEVEH
Empty for EKRON



82566 Max Power
3.3V : 28mA
1.8V : 440mA
1.0V : 297mA

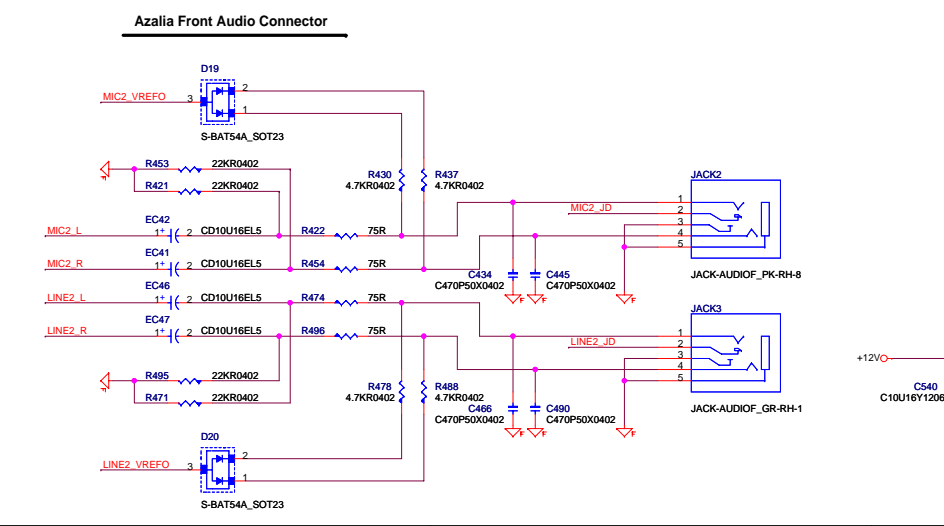
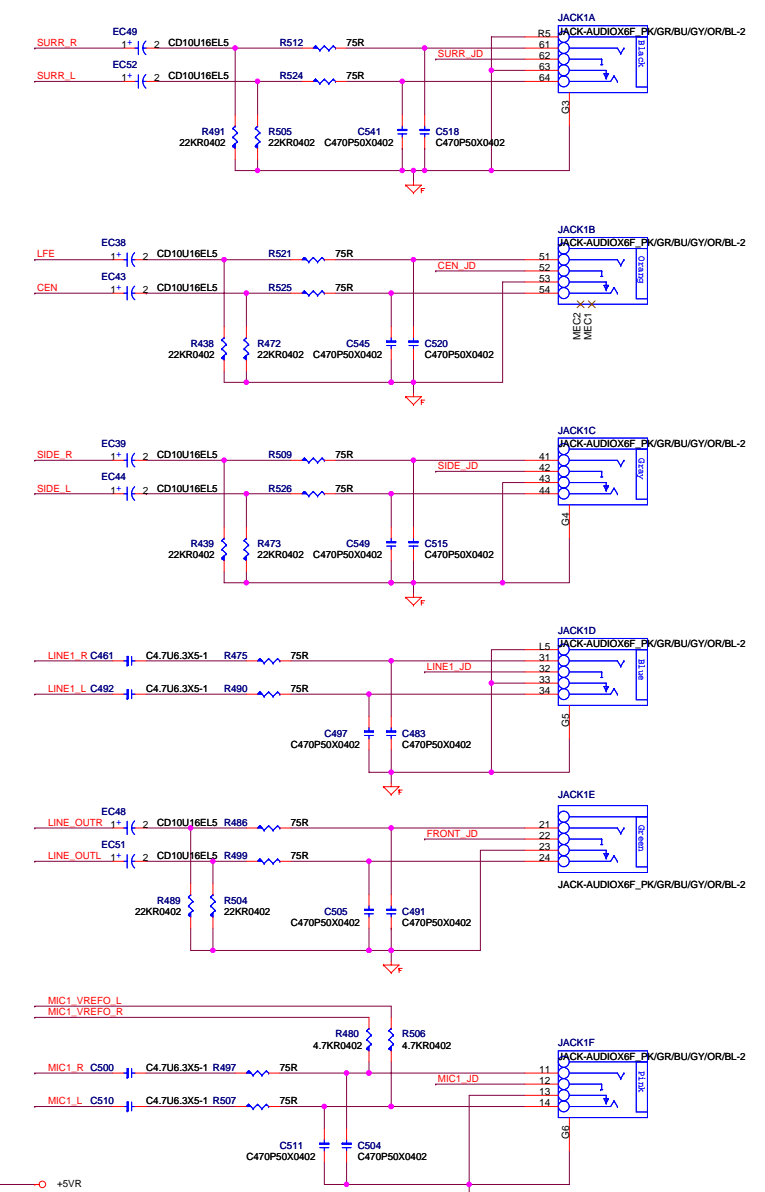
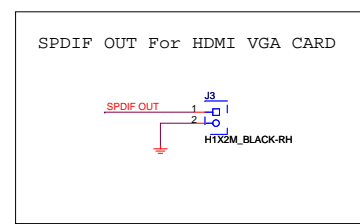
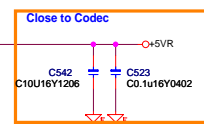
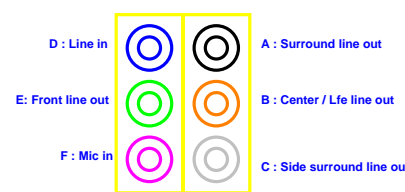
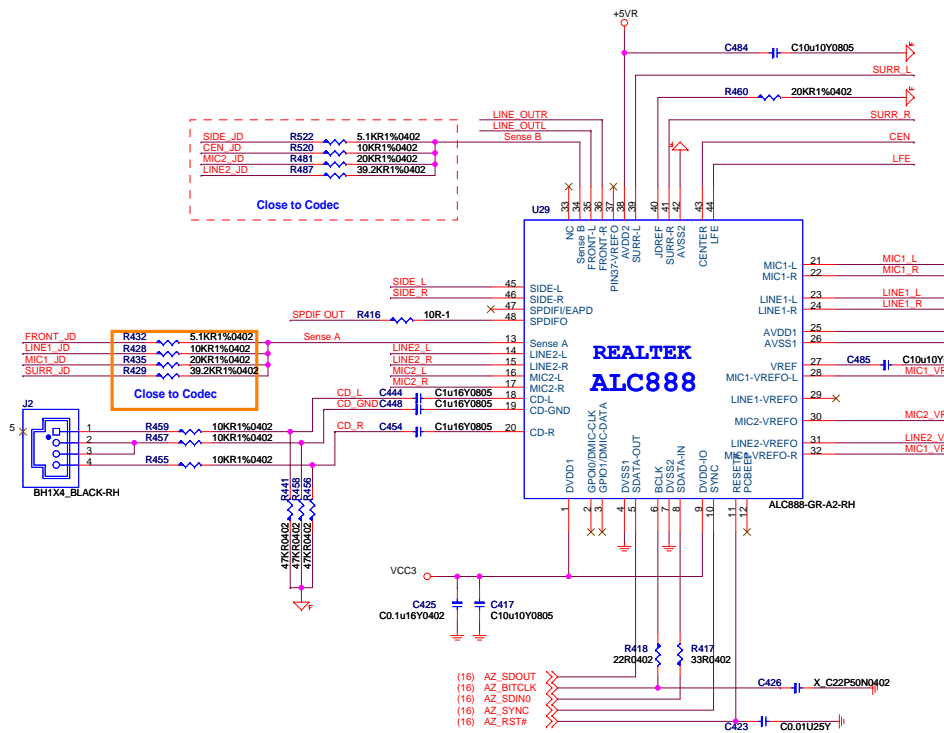


MODE_SEL R47 X 100R0402
Stuff for KUMERAN Only Mode
Empty for KUM+JORDAN Mode
STUFF STRAP FOR EKRON
EMPTY FOR NINEVEH

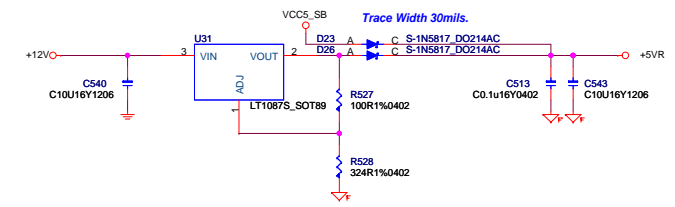


LED0# = Link 1000# (0111)
LED1# = Link/ACT# (0100)
LED2# = Link 100# (0110)

Micro Star Restricted Secret		
Title	PLC LAN 82566DC	Rev
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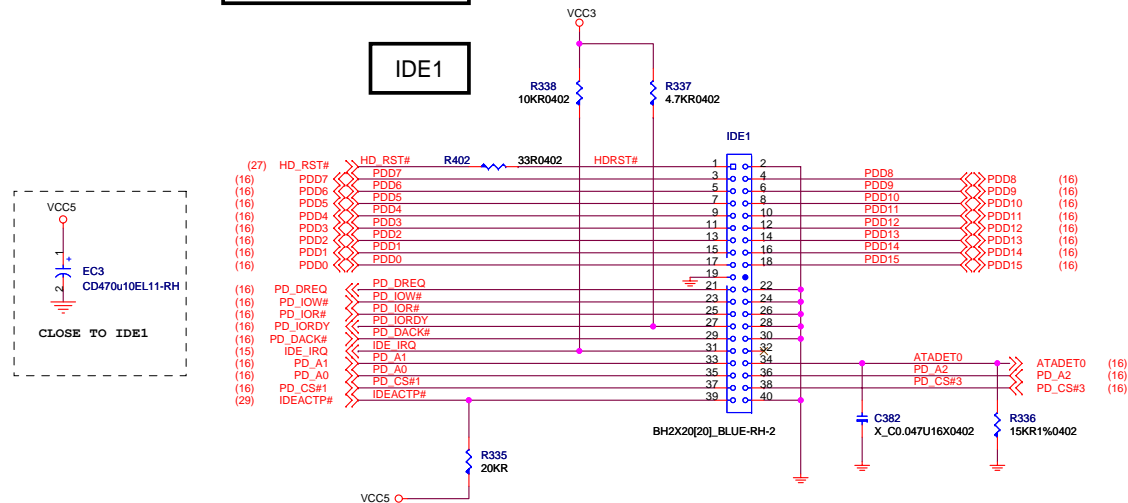
AUDIO CODE REGULATORS



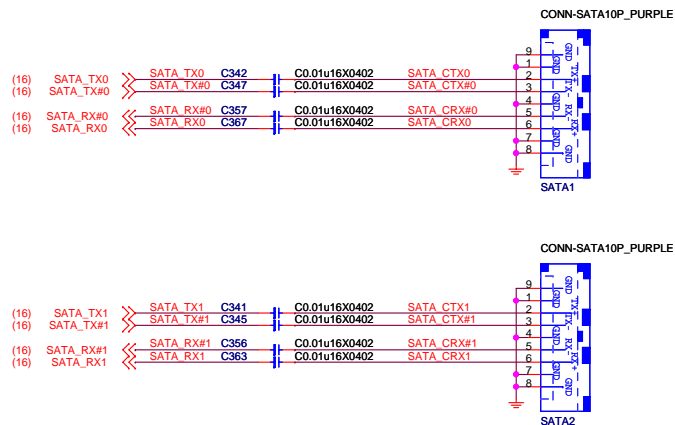
Micro Star Restricted Secret		
Title	Azalia CODEC ALC888	Rev 0A
Document Number	MS-7407	
MICRO-STAR INT'L CO.,LTD. No. 68, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, June 01, 2007
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IDE Connector

IDE1

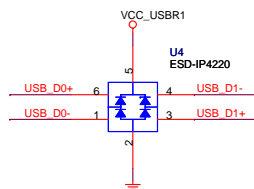
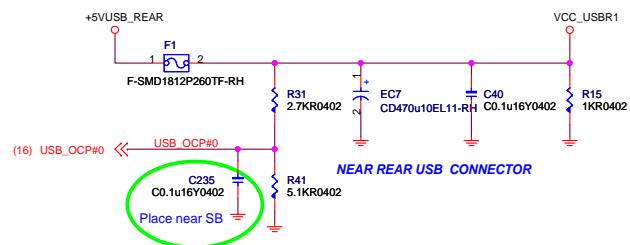


SATA CONNECTOR

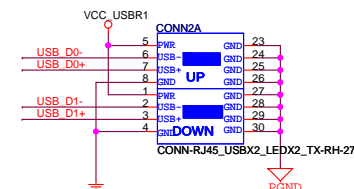
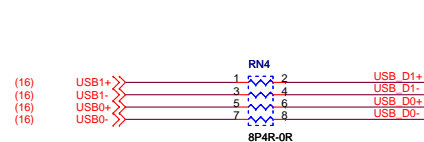


Micro Star Restricted Secret			
Title	IDE /SATA Connector		Rev
Document Number	MS-7407		0A
MICRO-STAR INT'L CO., LTD.		Last Revision Date:	
No. 66, Li-De St, Jung-Ho City,		Friday, June 01, 2007	
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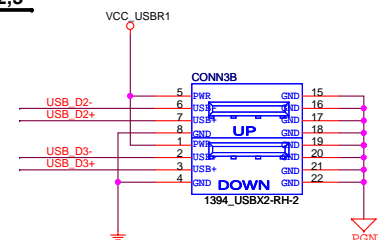
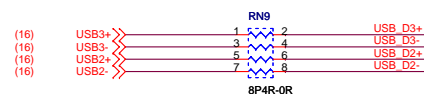
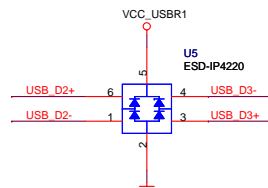
POWER CIRCUIT FOR USB PORT 0,1,2,3



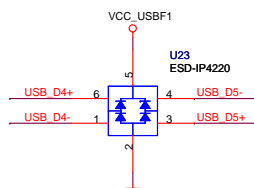
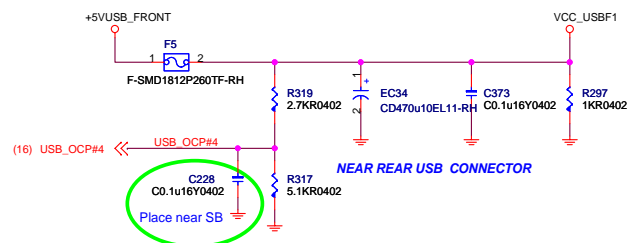
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



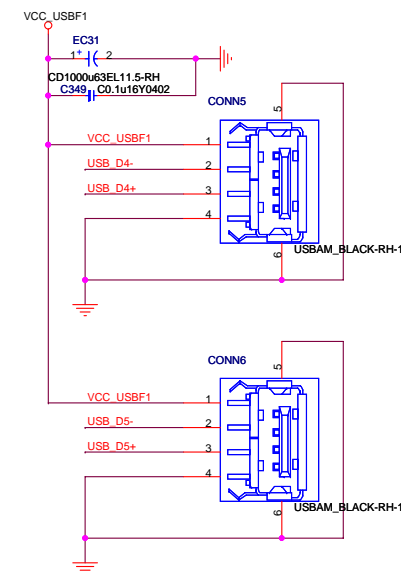
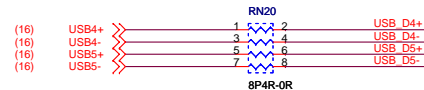
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



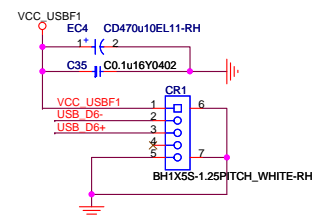
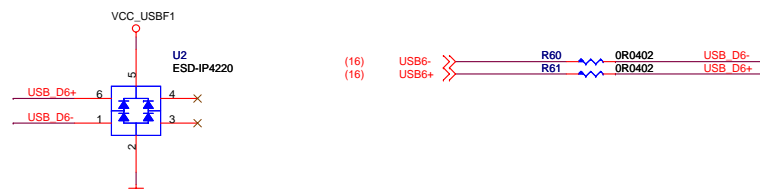
POWER CIRCUIT FOR USB PORT 4,5



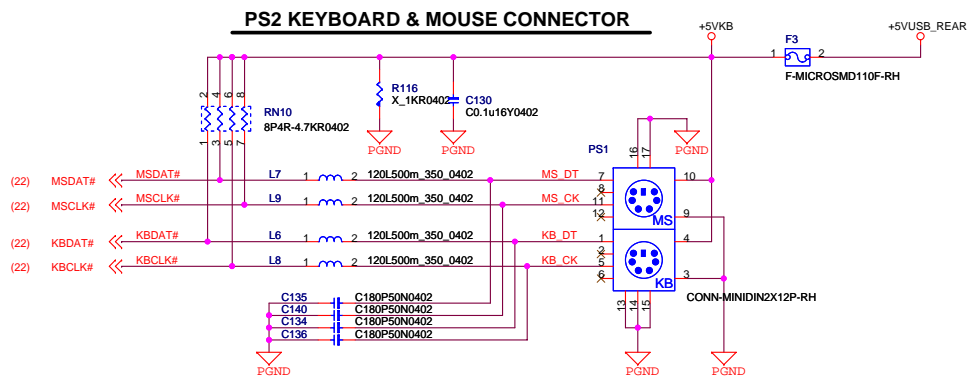
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



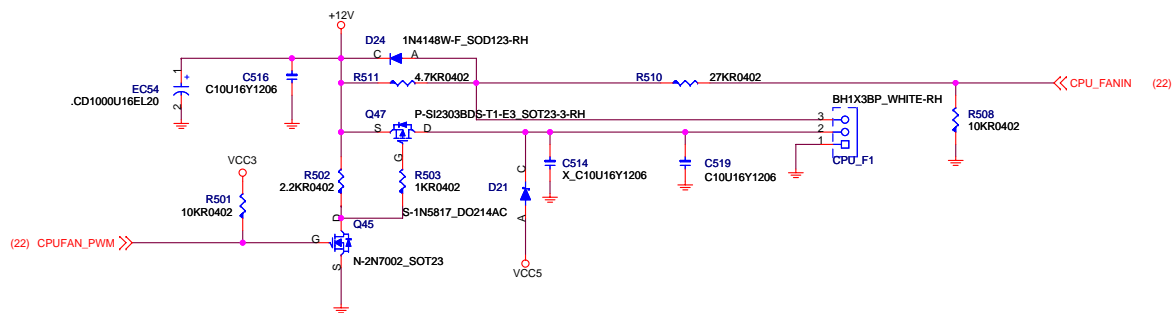
CARD READER USB CONNECTOR FOR USB PORT 6,



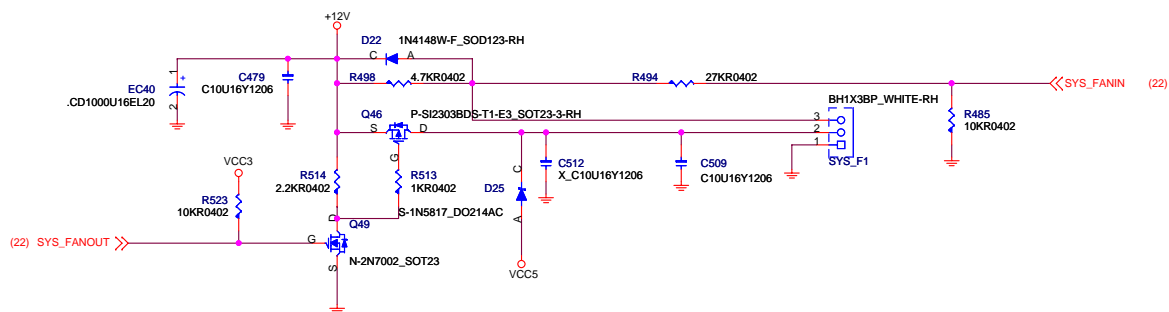
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Title	USB Connector	Rev
Document Number	MS-7407	0A
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CPU FAN

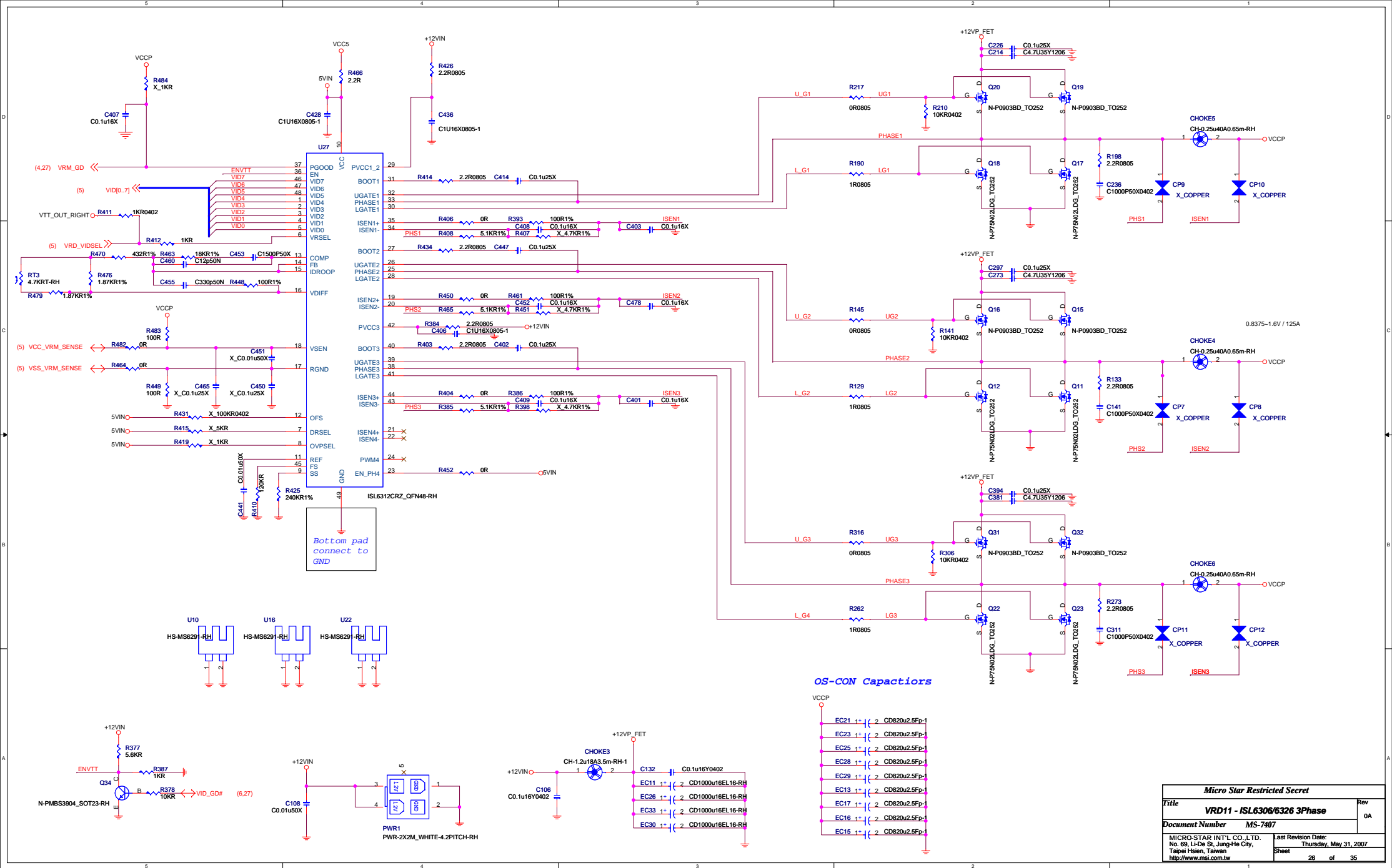


SYSTEM FAN



Micro Star Restricted Secret

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Document Number	MS-7407		
MICRO-STAR INT'L CO., LTD. No. 66, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, May 31, 2007 Sheet 25 of 35	



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Document Number	MS-7407	
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ACPI Controller MS-7

VDIMM LINEAR OR PWM SELECT

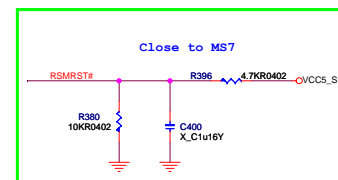
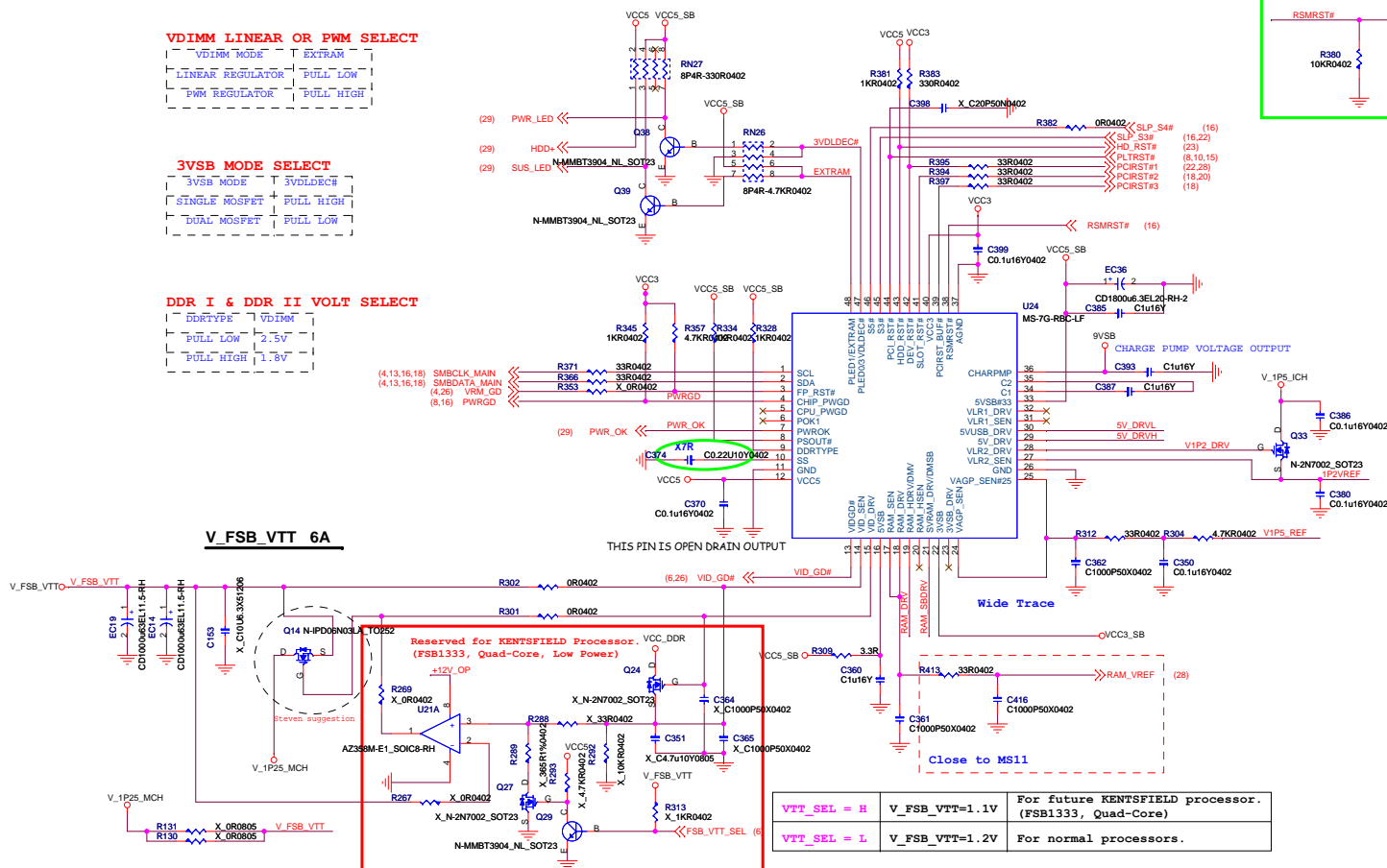
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

3VSB MODE SELECT

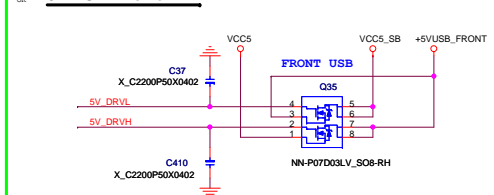
3VSB MODE	3VSDRIVE
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

DDR I & DDR II VOLT SELECT

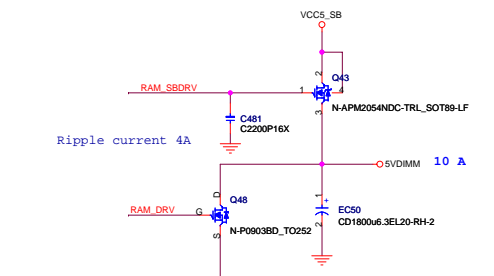
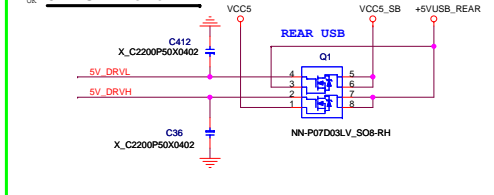
SDRTP#	VDIMM#
PULL LOW	2.5V
PULL HIGH	1.8V



5V DUAL Power 2A



5V DUAL Power 2A

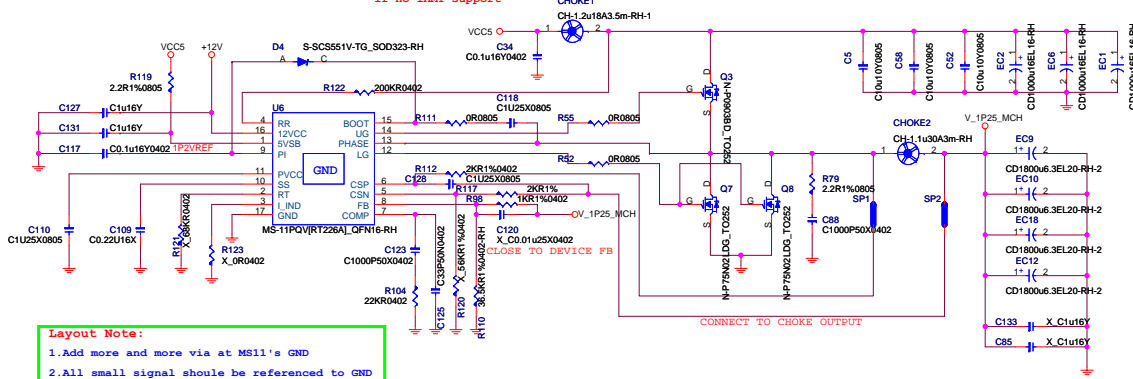


V_1P25_CORE POWER...28A

*Short to V_1P25_CL if no iAMT support

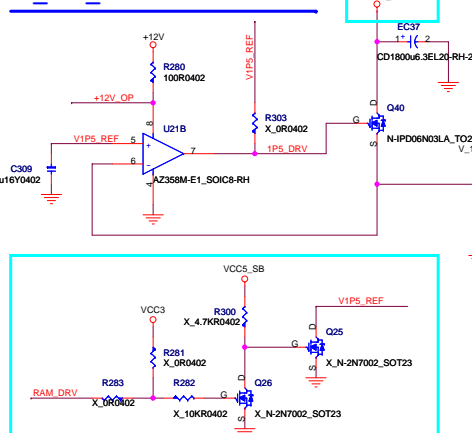
Note: Iripple=Iout*[D/N-(D*D)]^0.5...D=Vout/Vin

Iripple=25*0.48=12A
(2.35*2)*1.7=7.99A<12A

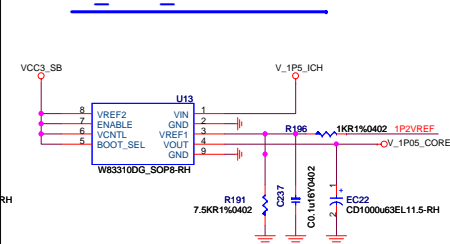


Layout Note:
1. Add more and more via at MS11's GND
2. All small signal should be referenced to GND

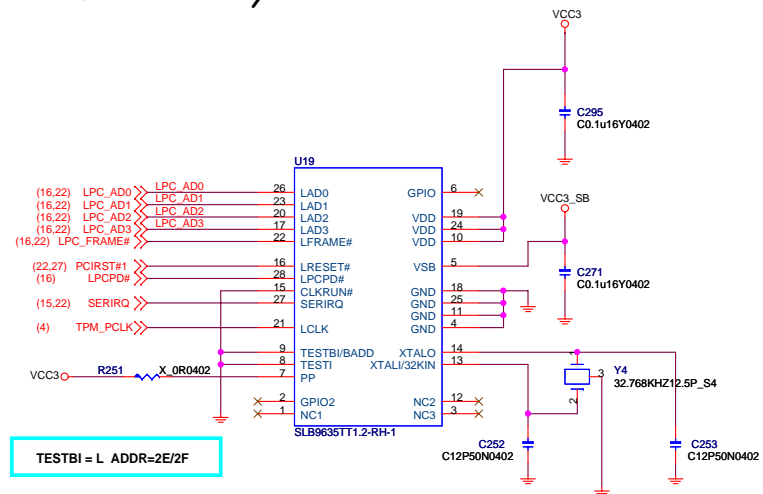
V_1P5_ICH...3A



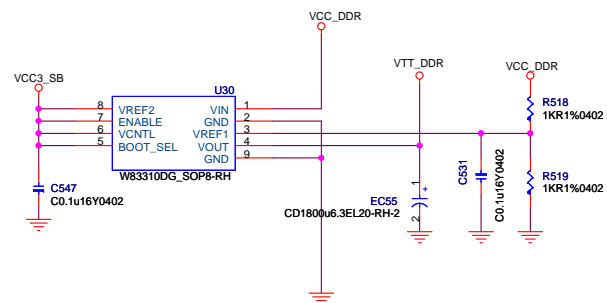
V_1P05_ICH...1.31A



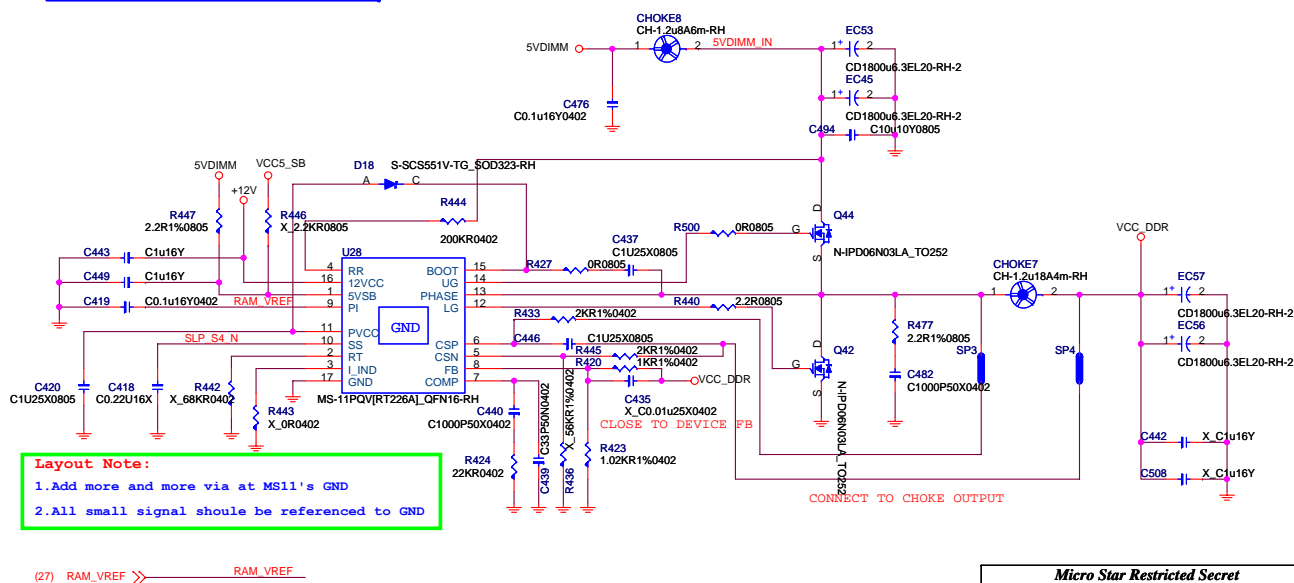
TPM - Security Controller



DDR II VTT POWER

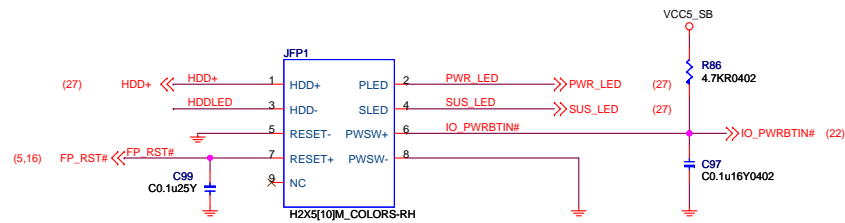


DDR II 1.8V POWER...16A

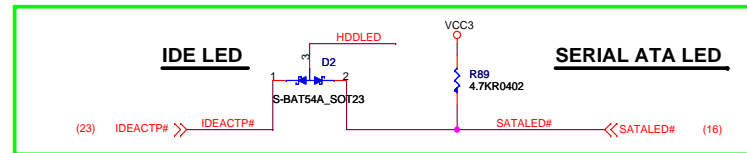
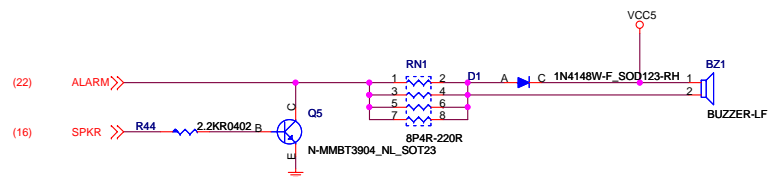


Micro Star Restricted Secret		
Title	TPM & DDRII Power	Rev
Document Number	MS-7407	0A
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Friday, June 01, 2007
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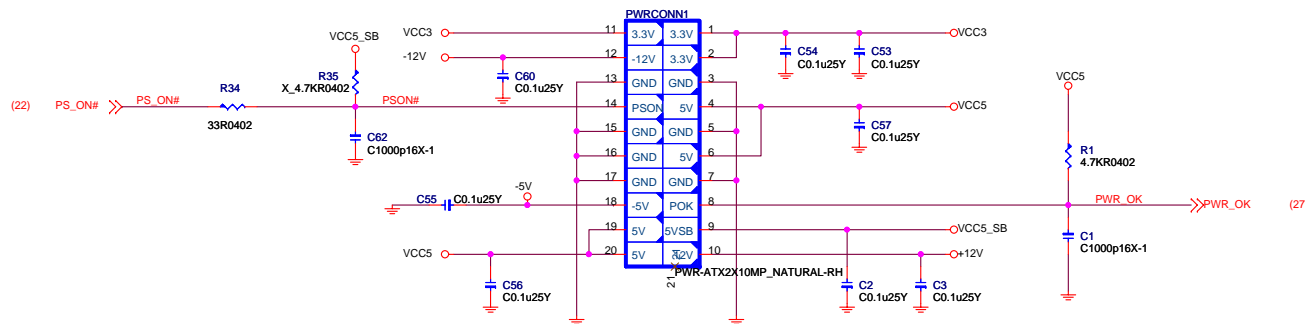
Intel Front Panel



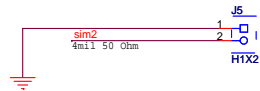
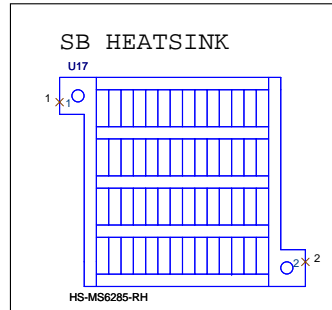
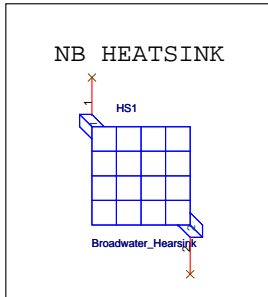
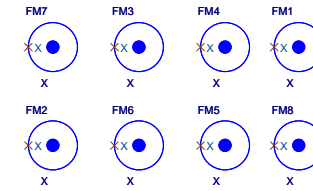
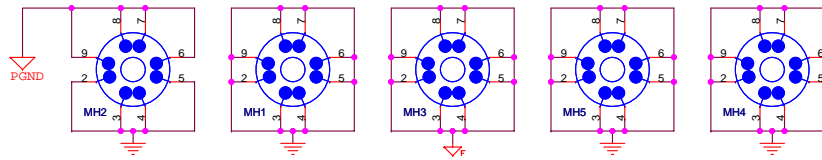
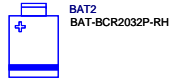
BUZZER



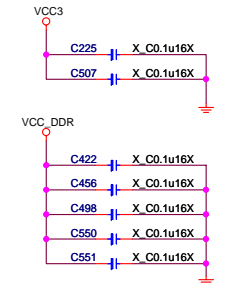
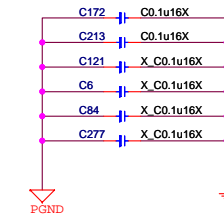
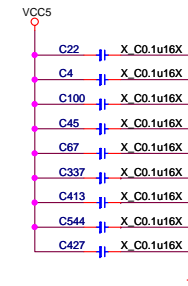
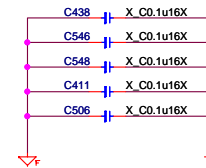
ATX



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Document Number	MS-7407	
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EMI



Micro Star Restricted Secret		
Title	Manual Parts	Rev 0A
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Title	Revision History	Rev
Document Number	MS-7407	0A
MICRO-STAR INT'L CO., LTD. No. 89, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, May 31, 2007 Sheet 31 of 35

LGA775 - CPU (65W)		
0.850V-1.3525V Core	-	125A
1.2V FSB VTT	-	5.3A

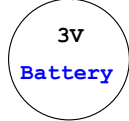
G31		
1.2V FSB_VTT	-	1.0A
1.25V Core	-	18.1A
1.25V DMI/PCI Exp.	-	2.5 A
1.8V VCC_DDR (S0,S1)	-	3.2A
1.8V VCC_SMCLK	-	250mA
3.3V VCCA_DAC	-	65.8mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	3.8A

ICH7		
1.05V Core	-	1.31A
1.5V DMI	-	40 mA
1.2V FSB_VTT	-	14 mA
1.5V_A USB/SATA	-	0.97A
1.5V_B PCI Exp.	-	0.74A
VCCRTC	-	6 uA
3.3V CL	-	12 mA
1.5V GbE LAN	-	74 mA
3.3V 10/100 LAN	-	12 mA
3.3V GbE LAN	-	1 mA
3.3V SusHDA	-	4 mA
3.3V HDA	-	24 mA
3.3V VccSus3_3	-	700mA
3.3V Vcc3_3	-	580mA

HD Audio ALC888		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

ICS9LP505		
3.3V VDD_48/PCI/REF	-	TBDA

INTEL 82566DC		
3.3V_SB I/O & LED	-	28mA
1.8V ANALOG	-	440mA
1.0V ANALOG	-	297mA



ISL6312		
VCCP	VRM 11	
0.850V-1.3525V		
3-Phase Switch	125A	

W83310DS		
VTT_DDR		
0.9V Linear	1.2A	

MS11+ Regulator		
VCC_DDR		
1.8V PWM		
9.4A+4.1A+2.5A	16A	

MS11+ Regulator		
V_1P25_MCH		
1.25V PWM		
20.6A+3.8A+6A	28A	

MS7 Regulator		
V_1P25_CL		
V_FSB_VTT		
1.2V Linear	6.3A	
V_1P5_ICH		
1.5V Linear	2A+1A	
V_1P05_ICH		
1.05V Linear	1.31A	
5V DUAL		
5V Switch	4A	
5VSB Switch	500mA	
5VDIMM		
5V Switch	6.2A	
5VSB Switch	500mA	

5VAUD	
5V	
500mA	

1.8V	
440mA	
1.0V	
297mA	

VCC5_SB	VCC5	VCC3_SB	VCC3	+12V
Switch	21.5A	Switch	8.4A	Switch
1A		1.5A		9.5A
ATX POWER CONN				

DDRII x2 & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x1		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB x7		
+5V (S0,S1)	-	3.5A
+5V (S3)	-	17.5mA

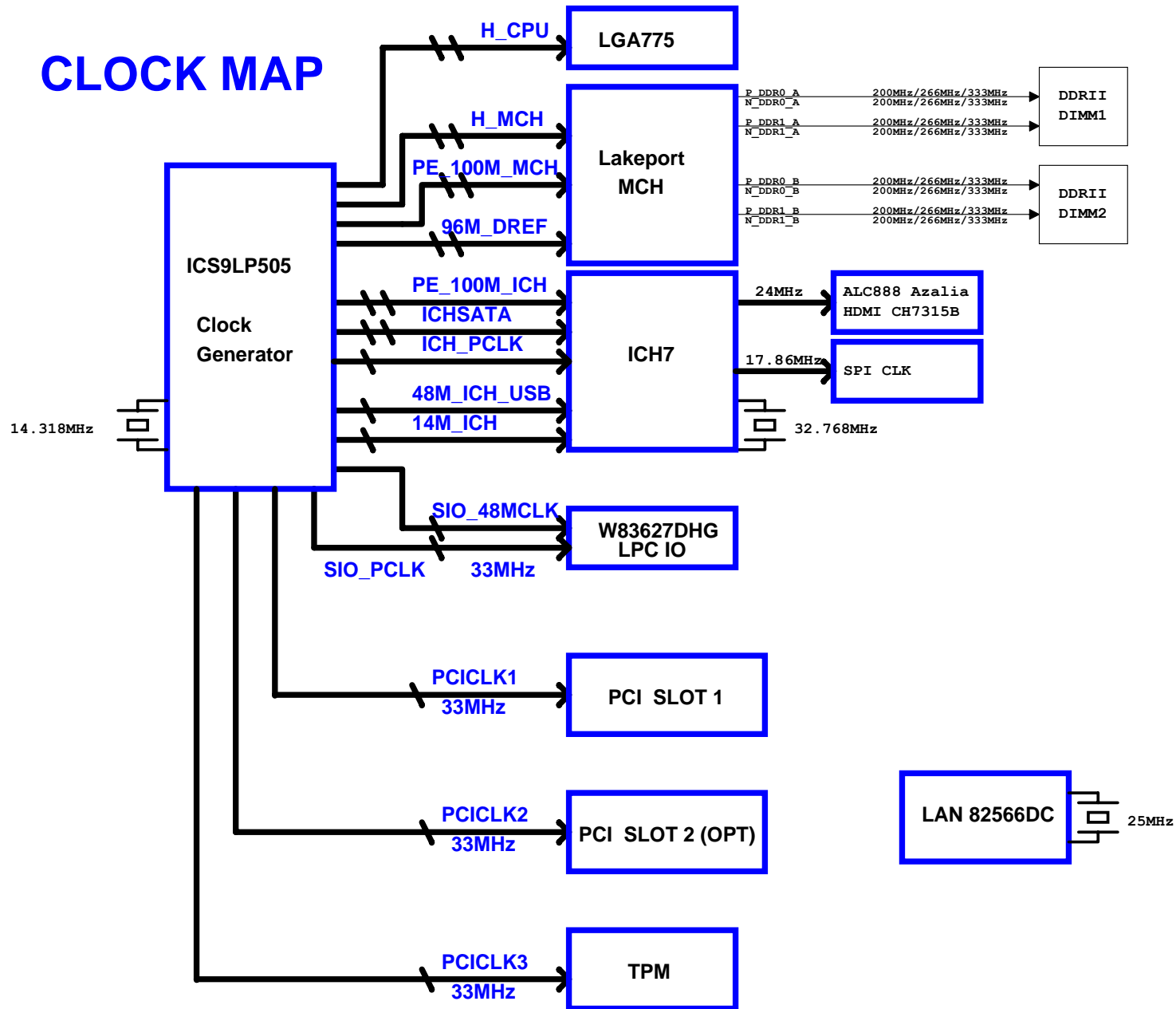
+12V CPU & SYS FAN		
	-	0.5A

DC 4Pin Output		
+12V		
+5V		

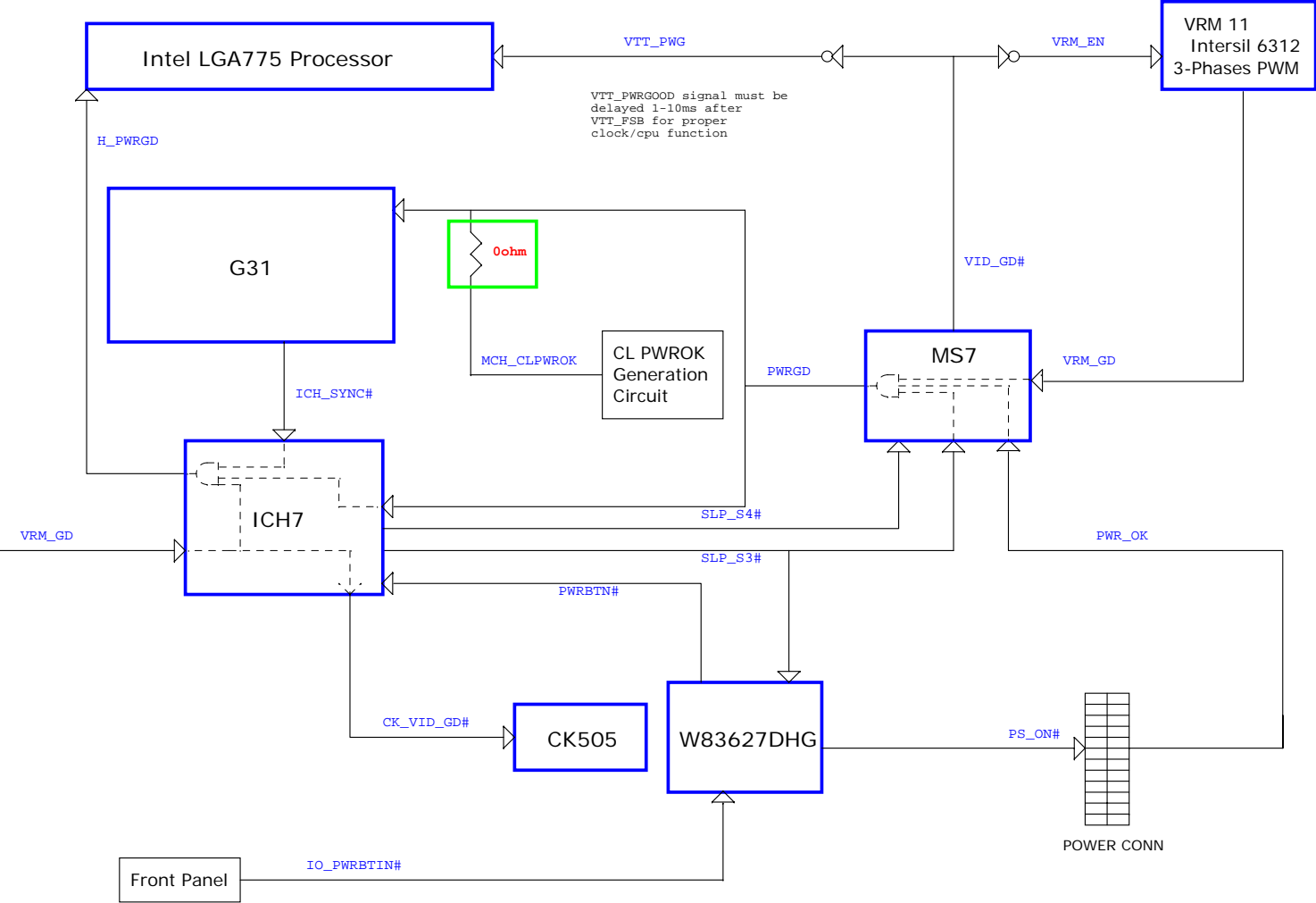
PS/2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

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Title	Power Delivery	Rev
Document Number	MS-7407	0A
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CLOCK MAP



PWROK MAP



RESET MAP

